

Application Note

June 16, 2005

AN1195.0

General Description

The EL1881 eval boards simplify the evaluation of the EL1883, a sync separator for both standard and non-standard video signal. It provides composite sync, vertical sync, burst/back porch timing, and odd/even field detection. For detail application, please refer to the EL1883 data sheet.

Features

- Fixed 70mV slicing of video input levels from 0.5V_{P-P} to 2V_{P-P}
- · Low 1.5mA supply current
- · Fully assembled and tested

Detailed Description

Value of R_{SET} and Low Pass Filter at the input

An external resistor R_{SET} that sets all internal timing. The demoboard is built with a $681 k\Omega$ resistor for standard NTSC and PAL video signals. If the input video signal is very noisy, a low pass filter is required at pin 2. In this case, R_F = 100 and C_F = 570pF provide a 2.79MHz LPF. This sufficiently

attenuates 3.58MHz or 4.43MHz color burst and passes the approximately 15.7kHz sync signals without appreciable attenuation. If the input video signal is clear, then simply just short the R_{F} and open C_{F} on the board.

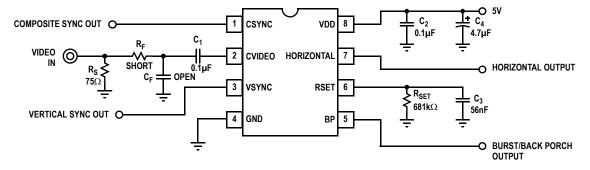
Layout Consideration

The PC board layout has been optimized for high-speed signals. Careful attention is given to the signal paths, power supply bypassing, and grounding. Small surface mount ceramic capacitors are placed as close as possible to the supply pins. To avoid noise problem, R_{SET} and C_{SEt} need to be placed close to the device.

Evaluation Set Up

- 1. Use a +5V supply. Connect the +5V to VDD pin and power supply ground to the GND pin.
- 2. Apply a NTSC or PAL video signal to V_{IN} BNC connector through a 75 Ω cable.
- 3. Use a $10M\Omega$ probe to check composite sync (CSYNC), vertical sync (VSYNC), burst/back porch timing (BP), and odd/even field detection (O/E).

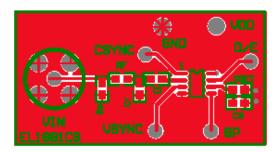
EL1883 Schematic

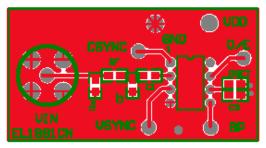


Bill of Materials

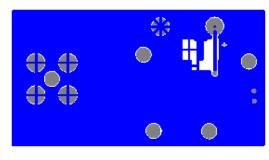
DESIGNATION	QTY	DESCRIPTION	MANUFACTURE	MFG. PART NUMBER
DUT	1	EL1883	Intersil	EL1883CS/CN
PCB	1	Printed Circuit Board, SOIC 8	DDI	EL1881 Demo Board
C1, C2	3	0.1µF, 10% Ceramic Capacitors	Vitramon	VJ0805Y104KXXA
C3	1	56nF, 10% Ceramic Capacitors		
C4	1	4.7μF, 10% Tantalum Capacitor	Vishay	293D475X9016B2T
R _S	1	75Ω, 1%	Dale	CRCW080575R0
R _F	1	0Ω, 1%	Dale	CRCW08050000
R _{SET}	1	681kΩ, 1%	Dale	
GND, VDD, CSYNC, VSYNC, O/E, BP	6	Printed Circuit Pin	Mill-max	3156-2-00-21-00-00-080
VIN	1	SMA 50Ω Straight Jack Connector	Johnson Components	98F1467

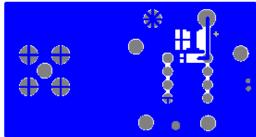
Eval Board Layouts (CS and CN package)





TOP LAYER





BOTTOM LAYER

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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